What is claimed is:

1. A power device comprising:

a semiconductor substrate having a first conductivity type;

a burying layer having a high concentration of a second conductivity type arranged deep in the semiconductor substrate;

a well having a low concentration of a second conductivity type formed on the burying layer of the semiconductor substrate;

a body region having a first conductivity type formed in a predetermined portion in the well having a low concentration of a second conductivity type;

first and second channel stop regions having a low concentration of a second conductivity type, the first channel stop region being formed in a predetermined portion of the body region and the second channel stop region being formed on at least one side of the body region having a first conductivity type;

a gate electrode including a gate insulating layer, formed on a space between the first and second channel stop regions;

source and drain regions having a high concentration of a second conductivity type formed in the first and second channel stop regions on both sides of the gate electrode; and

a body contact region formed in the source region;

wherein only the body region having a first conductivity type exists between the first and second channel stop regions, and a channel is formed between the first and second channel stop regions such that a uniform concentration can be obtained in a channel region.

2. The power device of claim 1, wherein the first and second channel stop regions are spaced apart from each other by a channel expected distance.

3. The power device of claim 1, wherein the first and second channel stop regions have a concentration higher than that of the well.

4. The power device of claim 3, wherein the first and second channel stop regions have enough low impurity concentration so that a desired breakdown voltage can be obtained.

5. The power device of claim 1, wherein the body region having a first conductivity type has a sufficient high impurity concentration so that punch-through can be prevented.

6. The power device of claim 1, wherein junction depths of the source and drain regions are the same as or smaller than those of the first and second channel stop regions.

7. The power device of claim 6, wherein the first and second channel stop regions have enough low impurity concentration so that a desired breakdown voltage can be obtained.

8. The power device of claim 1, wherein the first conductivity type is a p-type, and the second conductivity type is an n-type.

9. The power device of claim 1, wherein the gate insulating layer includes a fist gate insulating layer having a thin film and a second gate insulating layer having a thick film, which are connected to each other without cutting.

10. The power device of claim 9, wherein the gate electrode includes part of the first channel stop region, part of the body region, part of the second channel stop region, and part of the second gate insulating layer.

11. A method for manufacturing a power device, the method comprising:

forming a burying layer having a high concentration of a second conductivity type deep in a semiconductor substrate having a first conductivity type;

forming a well having a low concentration of a second conductivity type on the burying layer having a high concentration of a second conductivity type of the semiconductor substrate;

forming a body region having a first conductivity type in the well;

forming first and second channel stop regions having a low concentration of a second conductivity type in the center and on both edges of the body region;

forming a gate electrode between the first and second channel stop regions;

forming source and drain regions having a high concentration of a second conductivity type in the first and second channel stop regions on both sides of the gate electrode; and

forming a body contact region having a first conductivity type in the source region.

12. The method of claim 11, wherein the first conductivity type is a p-type, and the second conductivity type is an n-type.

13. The method of claim 12, wherein the forming of the body region and the forming of the first and second channel stop regions comprise:

implanting p-type impurities for a body region into a predetermined portion of the well;

implanting n-type impurities for first and second channel stop regions into a predetermined region of the well; and

activating the p-type and n-type impurities.

14. The method of claim 13, wherein the implanting of p-type impurities for a body region is performed by implanting boron (B) ions with a concentration of about 1 x 10^{13} to about 2 x 10^{13} atoms/cm^2.

15. The method of claim 13, wherein the implanting of n-type impurities

for first and second channel stop regions is performed by implanting arsenic (As) ions with a concentration of about 2 x 10^{13} to about 4 x 10^{13} atoms/cm^2.

16. A transistor, comprising:

a substrate having a first conductivity type containing a well having a low concentration of a second conductivity type;

a body region having a first conductivity type formed in a portion of the well; and

first and second channel stop regions having a low concentration of a second conductivity type, the first channel stop region formed in a portion of the body region and the second channel stop region formed on a side of the body region;

wherein a channel with a substantially uniform impurity concentration is located between the first and second channel stop regions.

17. The transistor of claim 16, further comprising a buried layer with a high concentration of a second conductivity type located between the substrate and the well.

18. The transistor of claim 16, further comprising source and drain regions having a high concentration of a second conductivity type formed in the first and second channel stop regions.

19. The transistor of claim 16, wherein only the body region exists between the first and second channel stop regions.

20. The transistor of claim 16, wherein the first and second channel stop regions have a concentration higher than that of the well.

21. The transistor of claim 20, wherein the first and second channel stop regions have a concentration low enough so that a desired breakdown voltage can be obtained.

22. The transistor of claim 16, wherein the body region has a concentration so that punch-through can be reduced.

23. A method for making a transistor, comprising:

providing a substrate having a first conductivity type containing a well having a low concentration of a second conductivity type;

providing a body region having a first conductivity type in a portion of the well; and

providing first and second channel stop regions having a low concentration of a second conductivity type, the first channel stop region provided in a portion of the body region and the second channel stop region provided on a side of the body region;

wherein a channel with a substantially uniform impurity concentration is provided between the first and second channel stop regions.

24. A method for making a power device, the method comprising:

providing a substrate with a first conductivity type;

forming a well with a low concentration of a second conductivity type in a portion of the substrate;

forming a body region with a first conductivity type in a portion of the well;

forming a first channel stop region with a low concentration of a second conductivity type in the body region; and

forming a second channel stop region with a low concentration of a second conductivity type immediately adjacent one side of the body region.

25. The method of claim 24, wherein a channel with a substantially uniform impurity concentration is provided between the first and second channel stop regions.